iC-PR Series
REFLECTIVE OPTO ENCODERS

preliminary

iC-Haus

FEATURES

♦ Lensless, reflective opto-encoder iCs, compact, high-resolution, incremental

♦ Suitable reflective code discs of $\varnothing$ 4, $\varnothing$ 14, $\varnothing$ 26 and $\varnothing$ 43 mm and linear scales with 256 µm period length

♦ Monolithic *HD Phased Array* with excellent signal matching

♦ Integrated blue LED with power control, *EncoderBlue®*

♦ Low-noise signal amplifiers with high EMI tolerance

♦ Pin-selectable modes of operation:
Digital A/B/Z (x1, x2, x4, x8, x16 interpolated),
analog COS/SIN with analog or digital Z

♦ Pin-selectable index gating:
Ungated (1 T), B-gated (0.5 T), AB-gated (0.25 T)

♦ Pin-selectable minimal edge distance: 80 ns, 1 µs, 10 µs

♦ Complementary quadrature outputs PA, NA, PB and NB

♦ Complementary index outputs PZ and NZ

♦ Analog signal output for ease of alignment and resolution enhancement by external interpolation

♦ Operating temperature range of -40 °C to +105 °C

♦ Compact and lensless optoQFN mold package

♦ Evaluation kits on request

APPLICATIONS

♦ Incremental encoders

♦ Miniature motors and actuators

♦ X-Y and linear stages

♦ Factory automation robots

♦ Consumer robots

PACKAGES
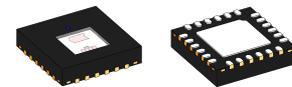
optoQFN24-4x4
4 mm x 4 mm x 0.9 mm

RoHS compliant

BLOCK DIAGRAM

iC-PR Series
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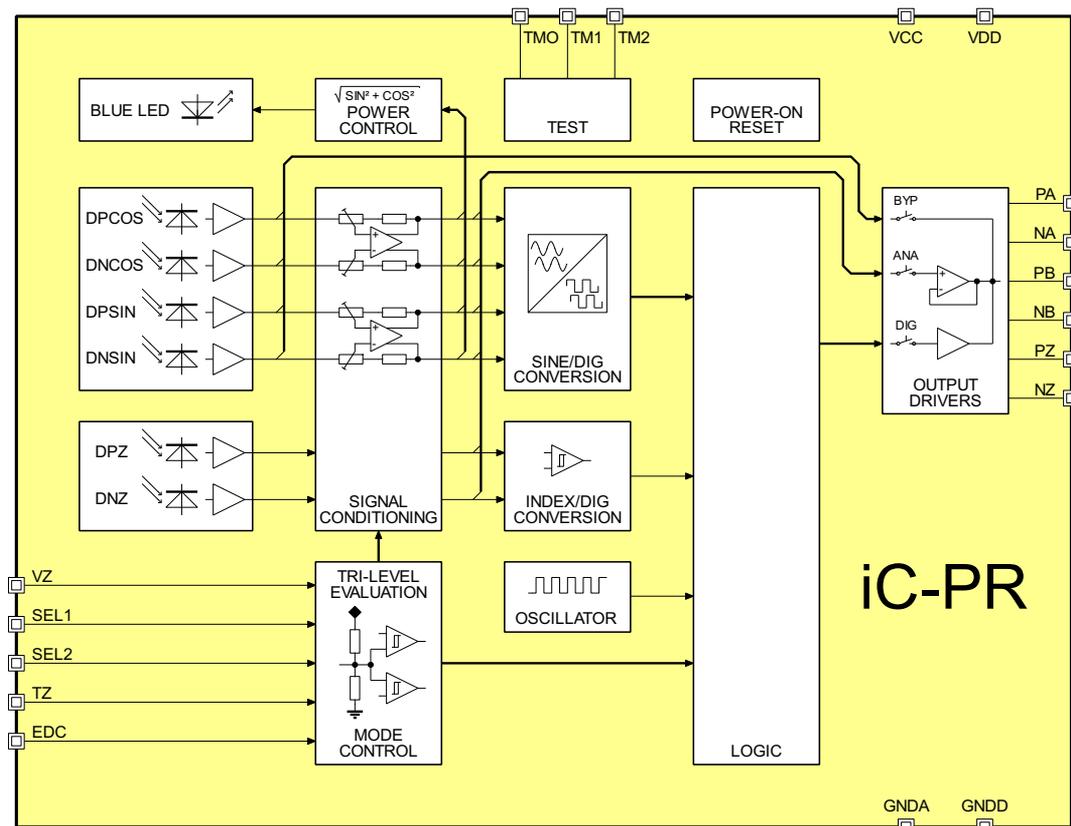
DESCRIPTION

The iC-PR series are advanced optical, reflective, lensless encoder iCs featuring integrated HD Phased Array photosensors and a blue LED. They provide high signal quality with relaxed alignment tolerances. Differential digital ABZ outputs with or without interpolation or analog SIN/COS outputs with index are available. Typical applications are incremental encoders for motor control.

Blue-enhanced photosensors are adapted to the short wavelength of the embedded blue LED, and provide low-jitter outputs due to improved signal contrast. The unique assembly technology of the blue LED emitter and sensors results in low optical crosstalk.

Low-noise transimpedance amplifiers, arranged in a paired layout to ensure excellent channel matching, are used to convert the sensor signals into voltages of several hundred millivolts.

Various operation modes are selectable via tri-level inputs SEL1 and SEL2: Digital outputs with native (x1) or interpolated resolution (x2, x4, x8 or x16), analog outputs or mixed analog/digital outputs, where the latter one combines analog COS/SIN signals with a digital index. The amplified analog output signals allow for inspection and monitoring of encoder assembly. Moreover, feeding external interpolation circuits (e.g. iC-NQ, iC-TW8 or iC-TW28) is possible.

Index gating is also pin-selectable via input TZ: The options are ungated (1 T), B-gated (0.5 T) or AB-gated (0.25 T).

Via tri-level input EDC a minimal edge distance of 80 ns, 1 µs or 10 µs can be preset for digital operation modes.

The devices feature a low power consumption. They run at single-sided analog supplies of 4.5 V up to 5.5 V and single-sided digital supplies of 3.0 V up to 5.5 V.

iC-PR4307
Code disc $\varnothing$: 43.0 mm
Optical radius: 19.8 mm
Native CPR: 720

iC-PR26xx
Code disc $\varnothing$: 26.0 mm
Optical radius: 10.8 mm
Native CPR: 250, 256, 360

iC-PR1456
Code disc $\varnothing$: 14.0 mm
Optical radius: 4.8 mm
Native CPR: 250, 256

iC-PR0464
Code disc $\varnothing$: 4.0 mm
Optical radius: 1.6 mm
Native CPR: 64

iC-PR256
Linear scale: 256 µm period length

PACKAGING INFORMATION

PIN CONFIGURATION
oQFN24-4x4 (4 mm x 4 mm)
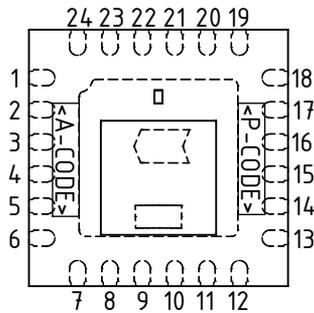
PIN FUNCTIONS

| No.	Name	Function
1	VDD	+3.0 V...+5.5 V Digital Supply Voltage
2	SEL1	Mode Selection Input 1
3	SEL2	Mode Selection Input 2
4	TZ	Index Gating Control Input
5	PZ	Index Output Z+
6	NZ	Index Output Z-
13	EDC	Edge Distance Control Input
14	NB	Incr. Output B- / Analog SIN-
15	PB	Incr. Output B+ / Analog SIN+
16	NA	Incr. Output A- / Analog COS-
17	PA	Incr. Output A+ / Analog COS+
18	GNDD	Digital Ground
19	GNDA	Analog Ground
20	TMO	Test Mode Output [2]
21	TM2	Test Mode Input 2 [2]
22	TM1	Test Mode Input 1 [2]
23	VZ	Index Detection Control Input
24	VCC	+4.5 V...+5.5 V Analog Supply Voltage
7..12	n.c.[1]	
	BP	Backside Paddle [3]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Pin numbers marked with n.c. are not connected.
2) The test pins may remain unconnected. TM1 and TM2 can be tied to GNDA to increase the noise immunity.
3) The backside paddle has to be connected by a single link to GNDA. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS

RECOMMENDED PCB-FOOTPRINT

3.80
2.49
R0.15
2.49
3.80
0.70
0.50

SIDE

0.15
0.90 ±0.10

TOP

4
1.78
1.78
4

BOTTOM

2.45
2.45
0.50
0.25
0.40
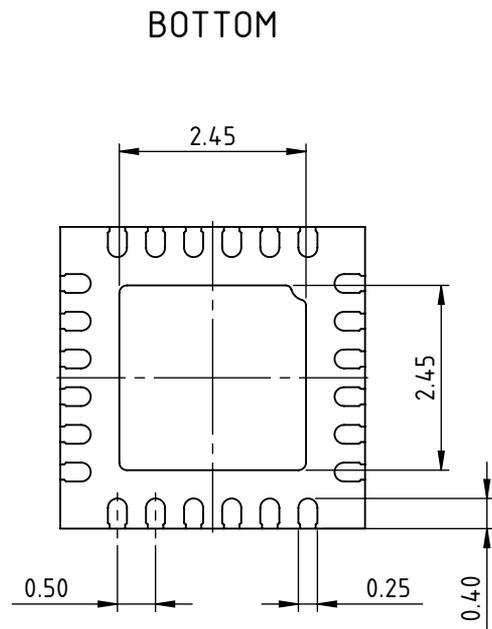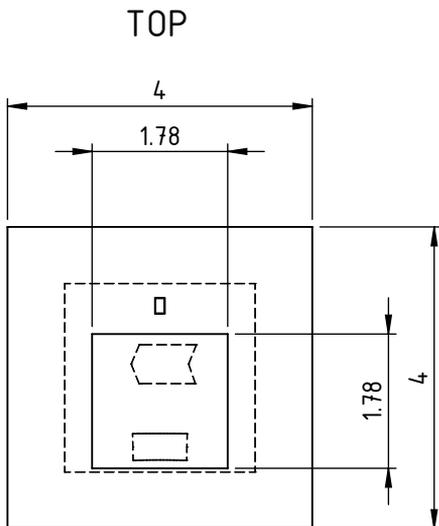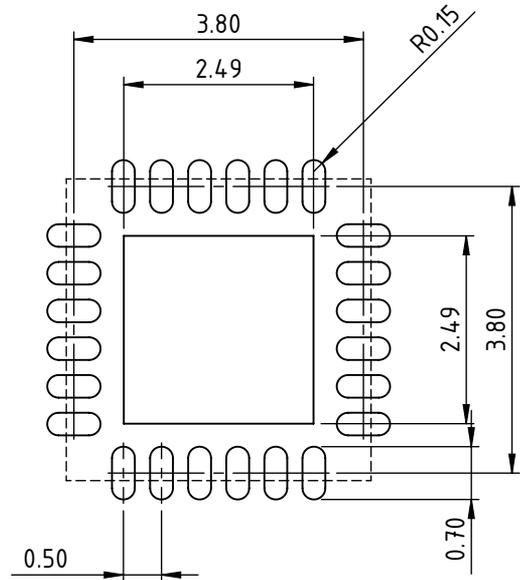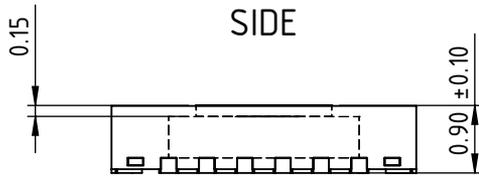
All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±1° (with respect to center of backside pad).
Maximum molding excess +20µm / -75µm versus surface of glass/reticle.

dra_prxxxx-oqfn24-1_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	120	mA
G003	VDD	Voltage at VDD		-0.3	6	V
G004	I(VDD)	Current in VDD		-20	120	mA
G005	V()	Pin Voltage, all signal outputs		-0.3	VCC + 0.3	V
G006	I()	Pin Current, all signal outputs		-20	20	mA
G007	Vd()	Electrostatic Discharge	Margin vs. ESD Susceptibility according to JEDEC, all pins [1,2]	2		
G008	Tj	Junction Temperature		-40	150	°C
G009	Ts	Chip Storage Temperature		-40	150	°C

[1] JEDEC document JEP 155: 500V HBM allows safe manufacturing with a standard ESD control process
[2] JEDEC document JEP 157: 250V CDM allows safe manufacturing with a standard ESD control process

THERMAL DATA

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		105	°C
T02	Tpk	Soldering Peak Temperature	tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor live 24 h at 30 °C and 60 % RH); Please refer to customer information file No. 7 for details.			245 230	°C °C
T03	Rthja	Thermal Resistance Chip to Ambient	package mounted on PCB according to JEDEC standard		50		W/K

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

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ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V, Tj = -40...105 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Analog Supply Voltage		4.5		5.5	V
003	VDD	Permissible Digital Supply Voltage	VDD ≤ VCC	3.0		5.5	V
004	I()	Supply Current	I(VCC)+I(VDD), Photocurrent Amplifiers within op. range, fout() <250 kHz, no load refer to Table 8 for details		20		mA
Photocurrent Amplifiers							
101	Z()	Equivalent Transimpedance Gain	Z() = Vout()/Iph(), Tj = 27 °C for PA, NA, PB, NB for PZ, NZ		4 6		MΩ MΩ
102	fc()hi	Cut-off Frequency (-3 dB)		200			kHz
Analog Outputs PA, NA, PB, NB, PZ, NZ							
201	Vout()ac	AC Signal Amplitude	Mode AAMP Mode A250 Mode A500DZ		250 250 500		mV mV mV
204	Vout()mx	Permissible Maximum Output Voltage	Mode AAMP			2.2	V
206	Vout()d	Dark Signal Level	Mode AAMP voltage at NZ voltage at PA, NA, PB, NB with no illumination T=-40 °C T=25 °C T=125 °C	870 780 640	980 880 765	1140 1060 940	mV mV mV
207	ΔVout()d	Dark Signal Matching of A, B	Mode AAMP, output vs. output	-2.5		2.5	mV
208	TCVout()d	Temperature Coefficient of Dark Signal Level	Mode AAMP voltage at NZ voltage at PA, NA, PB, NB with no illumination		-1.4		mV/K
209	VREF	Reference Voltage	Mode A250, A500DZ	48	50	52	%VCC
210	V()act	Signal Level at PZ-activation	V(PZ)act = V(NZ)-V(PZ) at activation see also Figure 1 refer to Table 8 for details		180 ..290		mV mV
211	I()mx	Permissible Load Current	Mode A250, A500DZ Mode AAMP	-1000 -100		1000 10	µA µA
212	C()mx	Permissible Capacitive Load				20	pF
Digital Outputs PA, NA, PB, NB, PZ, NZ							
401	fout()	Maximum Frequency per Output	Mode DX1, EDC low Mode DX2, EDC low Mode DX4, EDC low Mode DX8, EDC low Mode DX16, EDC low	0.2 0.4 0.8 1.6 1.85			MHz MHz MHz MHz MHz
402	AArel	AB Duty Cycle Variation	Mode DX1 Modes DX2, DX4, DX8, DX16 see also Figure 2	-5 -10		5 10	% %
403	HysD	Digital Hysteresis of Interpolator	Hysteresis with respect to one cycle of sine/cosine		5.6		°
404	Vs()lo	Saturation Voltage low	I() = 4 mA			0.4	V
405	Isc()lo	Short-Circuit Current low	V() = VDD	7		70	mA
406	Vs()hi	Saturation Voltage high	Vs()hi = VDD - V(), I() = -4 mA			0.4	V
407	Isc()hi	Short-Circuit Current high	V() = 0 V	-100		-7	mA
408	Tedc()	Edge Distance Control Time	EDC low EDC high EDC open	45 6600 640	80 10000 1000	135 14900 1520	ns ns ns
Tri-Level Programming Inputs SEL1, SEL2, EDC, TZ, VZ							
601	Vt()lo	Tri-Level Threshold Voltage low		10			%VCC
602	Vt()hi	Tri-Level Threshold Voltage high				90	%VCC

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V, Tj = –40...105 °C, unless otherwise noted

| Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
603	Vt()mid	Tri-Level Threshold Voltage mid		30		70	%VCC
604	V0()	Pin-Open Voltage		45	50	55	%VCC
605	Rpd()	Pull-Down Resistor	V() = VCC	65			kΩ
606	Rpu()	Pull-Up Resistor	V() = GNDA	65			kΩ
LED Power Control							
901	Iop()	Permissible LED Current		0.5		20	mA
902	Ictrl()	Controlled LED Output Current	refer to Table 8 for details		5 ..10		mA
Power-On Reset							
A01	VCCon	Turn-on Threshold VCC (power-on release)	increasing voltage at VCC VDD > VDDon, LED Current and Photocurrent Amplifiers within op. range			3.95	V
A02	VCCoff	Turn-off Threshold VCC (power-down reset)	decreasing voltage at VCC VDD > VDDon, LED Current and Photocurrent Amplifiers within op. range	3.00			V
A03	VCChys	Threshold Hysteresis VCC	VCChys = VCCon - VCCoff		220		mV
A04	VDDon	Turn-on Threshold VDD (power-on release)	increasing voltage at VDD VCC > VCCon, LED Current and Photocurrent Amplifiers within op. range			2.95	V
A05	VDDoff	Turn-off Threshold VDD (power-down reset)	decreasing voltage at VDD VCC > VCCon, LED Current and Photocurrent Amplifiers within op. range	2.3			V
A06	VDDhys	Threshold Hysteresis VDD	VDDhys = VDDon - VDDoff	200			mV

**ELECTRICAL CHARACTERISTICS: Diagrams**
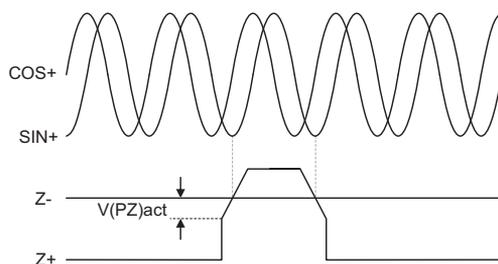
Figure 1: Z-signal level definition.
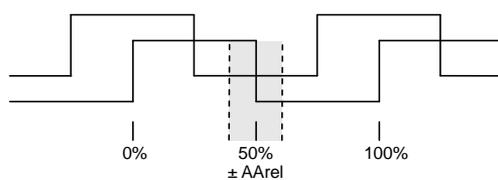
Figure 2: Definition of AB duty cycle variation.

SIGNAL DEFINITIONS
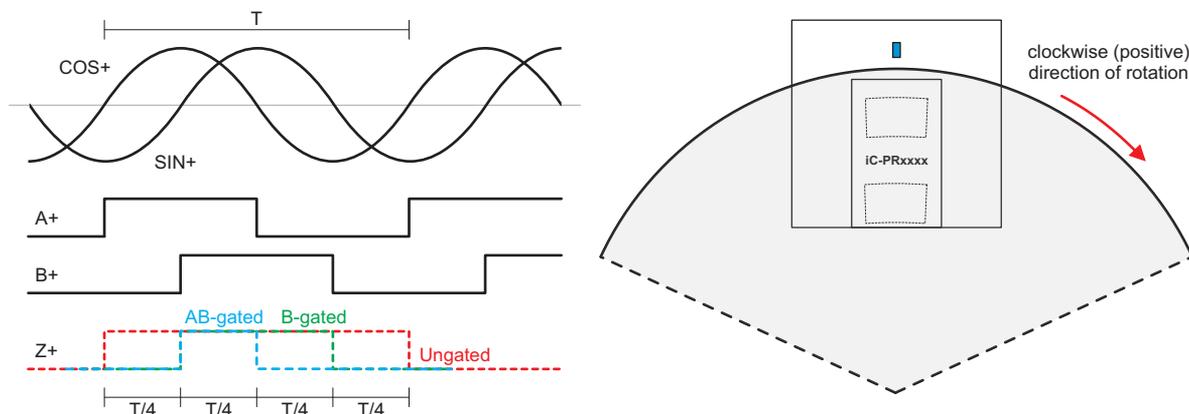
Figure 3: Signal definitions for clockwise (positive) direction of rotation.
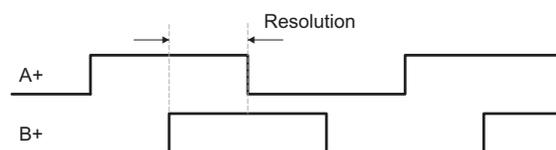
Figure 4: Definition of resolution for linear series.

OPERATION MODES

The iC-PR series features 8 principle operation modes, which are selectable by the voltages applied to the pins SEL1 and SEL2, as summarized in Table 4.

These tri-level inputs might be connected to a voltage below Vt()lo (low, see 601), a voltage above Vt()hi (high, see 602) or a voltage between the specified values of Vt()mid (open, see 603). For other voltages the function is undefined.

The open configuration can be easily obtained by an external voltage divider. Alternatively, when the pin is left unconnected, the iC itself biases the input at 50% VCC (see 604).

Note: Static pin voltages at SEL1 and SEL2 are required during operation. If changing the setting of SEL1 and SEL2 pins during operation, power-on reset of iC-PR is required.

SEL1	SEL2	Mode	Description
low	high	DX1	digital A/B/Z (x1 interpolation)
high	low	DX2	digital A/B/Z (x2 interpolation)
low	open	DX4	digital A/B/Z (x4 interpolation)
high	high	DX8	digital A/B/Z (x8 interpolation)
high	open	DX16	digital A/B/Z (x16 interpolation)
open	low	A250	analog COS/SIN (VREF $\pm$ 250 mV), analog Z, see Figure 5
open	high	AAMP	analog COS/SIN (transimpedance amps. $\pm$ 250 mV), analog Z, see Figure 5
open	open	A500DZ	analog COS/SIN (VREF $\pm$ 500 mV), digital Z (ungated), see Figure 5

Table 4: Operation modes selectable by pins SEL1/2.

ANALOG / MIXED OPERATION MODES
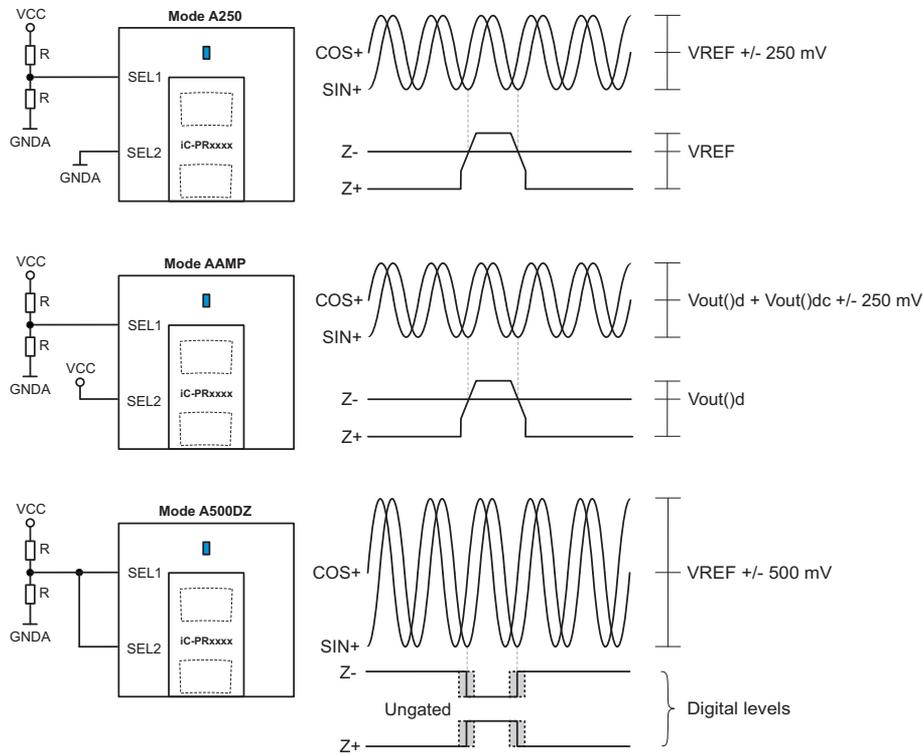
Figure 5: Analog / mixed operation modes. Complementary signals COS- and SIN- not shown.

Vout()d is the dark signal level of the analog signals. It is independent of illumination but proportional to temperature.

Vout()dc is the dc-level of the analog signals with respect to the dark signal level. It is proportional to illumination but independent of temperature.

## DIGITAL OPERATION MODES

INTERPOLATION FACTOR AND INDEX GATING
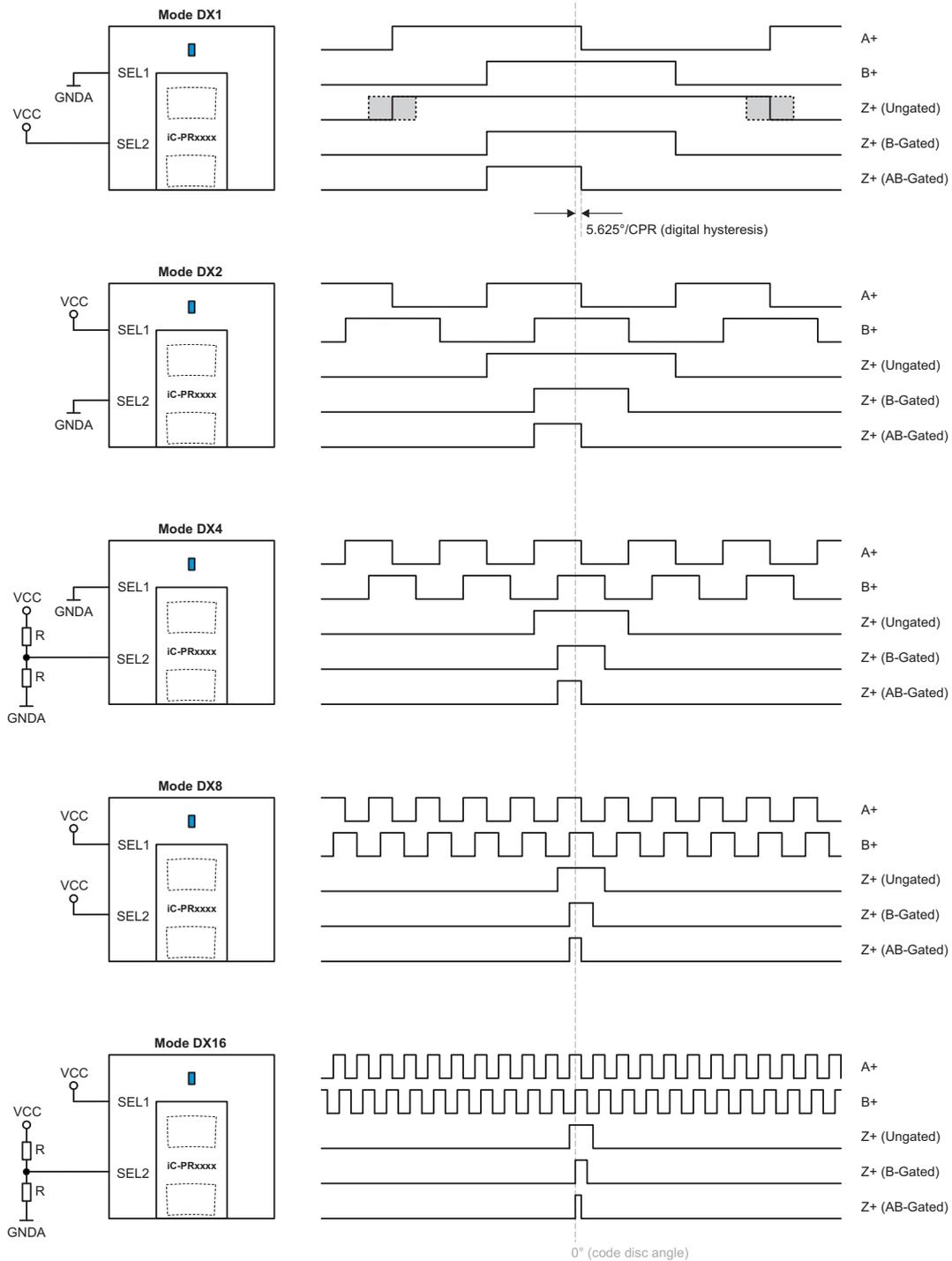
Figure 6: Digital operation modes (interpolation and index gating). Complementary signals A-, B- and Z- not shown.

An overview of the digital modes (interpolation and index gating) is depicted in Figure 6. The index gating can be controlled via tri-level pin TZ, as defined by Table 5.

Note: Static pin voltage at TZ is required during operation.

TZ	Description
low	B-gated index (180°)
high	Ungated index (360°)
open	AB-gated index (90°)

Table 5: Index gating controlled by pin TZ.

DIGITAL HYSTERESIS

In all interpolation modes the iC-PR series features a digital angular hysteresis of $\frac{360°}{64 \cdot CPR}$, i.e. 1 LSB of the angular resolution in mode DX16. As illustrated in Figure 7, the digital hysteresis corresponds to a slip existing between the two rotating directions. In this way multiple switching of the incremental signals at the reversing point of a changing direction of rotation is prevented.
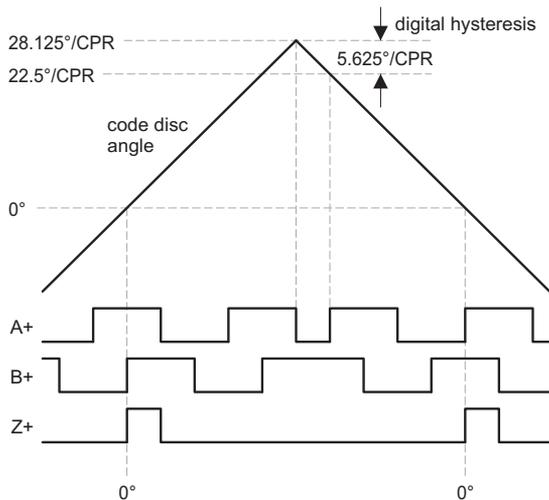
Figure 7: Digital hysteresis in mode DX16 with AB-gated index.

EDGE DISTANCE CONTROL

With the tri-level input pin EDC a minimal edge distance of 80 ns, 1 µs or 10 µs (typical values) can be configured to suit the system on hand (cable length, external counter). It is recommended to set EDC low.

Note: Static pin voltage at EDC is required during operation.

EDC	Description
low	80 ns minimal edge distance
high	10 µs minimal edge distance
open	1 µs minimal edge distance

Table 6: Minimal edge distance controlled by pin EDC.

STARTUP BEHAVIOR

When iC-PR is powered on, the digital outputs are held in a defined state:

$$PA = NA = PB = NB = low$$
$$PZ = NZ = high$$

This specific combination of output signal levels is invalid during normal operation, hence signalizing that the iC is in the startup phase. Once the logic has found and verified the code disc position, valid A/B/Z signals are then output henceforth.

Note: iC-PR will also enter or remain in the startup state, when the regulated LED current exceeds a specific value, e.g. due to code disc misalignment. Once the LED current returns to a valid range, the logic will again search for the code disc position and output valid A/B/Z signals afterwards.

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INDEX DETECTION THRESHOLD

Via tri-level pin VZ an internal threshold for the index detection can be controlled, as described in Table 7. Setting VZ low (maximal threshold), a safe detection of the index pulse requires stronger illumination of the respective photodiodes, which also results in a stronger interference resistance against extraneous or stray light. On the other hand, with VZ high (minimal threshold) less illumination of the index photodiodes is required for a safe detection. However, in this case the interference resistance is reduced respectively. With VZ open the threshold lies in between the other two options.

For working distances above 1.5 mm (IC to code disc), the recommended value for VZ is shown in Table 8. For smaller working distances, it may be necessary to decrease the index detection threshold.

VZ	Description
low	Maximal threshold
high	Minimal threshold
open	Medium threshold

Table 7: Index detection controlled by pin VZ.

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DEVICE OVERVIEW

Device	CPR	Code Disc		Supply Current / mA		Max. RPM		VZ	Activ. Level
	native	P/O Code	Type	1.5 mm[1]	2.0 mm[1]	DX1/2/4/8	DX16	$\geq$1.5 mm[1]	V(PZ)act / mV
∅ 43 Series									
iC-PR4307	720	PR08PS	M	21	27	16000	9000	low	290
∅ 26 Series									
iC-PR2604	360	PR04PS	M	21	26	32000	18000	low	290
iC-PR2656	256	PR05PS	M	16	18	45000	25000	open	280
iC-PR2656	250	PR10PS	M	16	18	45000	25000	open	280
∅ 14 Series									
iC-PR1456	256	PR07PS	M	21	27	45000	25000	high	180
iC-PR1456	250	PR09PS	M	21	27	45000	25000	high	180
∅ 04 Series									
iC-PR0464	64	PR06PS	P	21	27	180000	100000	high	200

Device	Res.	Code Disc		Supply Current / mA		Max. Speed / m/s		VZ	Activ. Level
	DX16	P/O Code	Type	1.5 mm[1]	2.0 mm[1]	DX1/2/4/8	DX16	$\geq$1.5 mm[1]	V(PZ)act / mV
Linear Series									
iC-PR256	4 µm	PR01L	P	16	18	50	28	low	290

Type M = Makrolon
Type P = Polycarbonate

Definition of resolution for linear series see Figure 4.

Device availability on request.

Table 8: Device overview

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[1] Working distance iC to code disc.

APPLICATION NOTES

Application notes for iC-PR-series devices are shown separately.

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A2.0	2016-03-31	BLOCK DIAGRAM	Block diagram updated.	1
		ELECTRICAL CHARACTERISTICS	204, 212: Moved value from "min." to "max." as defined as "permissible"	6
		SIGNAL DEFINITIONS	Figure for definition of resolution in linear series added.	9
		OPERATION MODES	Description of analog modes in Table 4 updated.	9
		DIGITAL OPERATION MODES	Recommended EDC configuration added.	12
		INDEX DETECTION THRESHOLD	Updated description.	13
		DEVICE OVERVIEW	Device overview table extended and updated. Changed recommendation for VZ.	14

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1.0	2015-11-23		Initial Release	all

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PRnnnn	24-pin optoQFN, 4 mm x 4 mm, 0.9 mm thickness RoHS compliant	nnnn = device version	iC-PRnnnn oQFN24-4x4
Evaluation kit	Kit with Reflective Encoder IC PR1M (61mm x 64 mm), Code Disc	nnnn = device version	iC-PRnnnn EVAL PR1M
Mother board	Adapter PCB (80 mm x 110 mm)	incl. ribbon cable	iC-PR EVAL PR2M

Please send your purchase orders to our order handling team:

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